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PATENT  
8008-1050

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Hiroyoshi KUGE et al. Conf. 3414

Application No. 10/786,552 Group 2825

Filed February 26, 2004

SEMICONDUCTOR INTEGRATED CIRCUIT  
DEVICE AND DESIGN AUTOMATION  
APPARATUS, METHOD AND PROGRAM

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the cited documents are made of record on the enclosed PTO Form-1449.

As the USPTO has waived the requirement under 37 CFR 1.98(a)(2)(i) for submitting a copy of each cited U.S. patent and patent publication for applications filed after June 30, 2003, copies of the cited U.S. references are not enclosed, as the present application is filed after June 30, 2003. Copies of the cited foreign patent documents and/or non-patent literature are enclosed.

A concise explanation of the relevance of these items is that these references were cited by the European Patent Office in the corresponding European Application Serial

Docket No. 8008-1050  
Appln. No. 10/786,552

No. 04004080.0-2216. A copy of the European search report in which they were cited is attached hereto.

Respectfully submitted,

YOUNG & THOMPSON



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Robert J. Patch, Reg. No. 17,355  
745 South 23<sup>rd</sup> Street  
Arlington, VA 22202  
Telephone (703) 521-2297  
Telefax (703) 685-0573  
(703) 979-4709

RJP/fb

August 26, 2004

INFORMATION DISCLOSURE CITATION <b>JTAG APPLICATION</b> <i>(Use several sheets if necessary)</i> AUG 26 2004			Attorney Docket No.: <b>8008-1050</b>	Application No.: <b>10/786,552</b>		
			Applicant: <b>Hiroyushi KUGE et al.</b>			
			Filing Date: <b>February 26, 2004</b>	Group Art Unit: <b>2825</b>		
<b>U.S. PATENT DOCUMENTS</b>						
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing date (if appropriate)
	2002/0004929	1/10/2002	Osaki et al.			
	6,145,116	11/7/2000	Tawada			
	5,509,019	4/16/1996	Yamamura			
<b>FOREIGN PATENT DOCUMENTS</b>						
Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes      No
	2000022081 (English abstract only)	1/21/2000	JAPAN			
	10144796 (with English abstract)	5/29/1998	JAPAN			X
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
	Jones, T.R.: "JTAG CLOCK & CONTROL SIGNAL DISTRIBUTION SCHEME" Motorola Technical Developments, Motorola Inc. Schaumburg, Illinois, US, vol. 18, 1 March 1993, pages 44-49					
EXAMINER:			DATE CONSIDERED			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.						

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\* Abstract provided for the Examiner's convenience